WHAT IS CLAIMED IS:

Claim 1 A frequency synthesizer apparatus comprising:

a voltage control oscillator operable to generate an output signal having a frequency corresponding to an input control voltage;

a variable frequency divider operable to divide the frequency of the output signal from said voltage control oscillator in accordance with an input data corresponding to a number of frequency division, and to output a frequency-divided signal;

a phase comparator operable to perform a phase comparison between the output signal from said variable frequency divider and an input reference signal, and to generate and output a signal indicating a result of the phase comparison;

a low-pass filter operable to low-pass-filter the output signal from said phase comparator, and to output the low-pass-filtered signal to said voltage control oscillator;

a fraction part control circuit operable to receive an input data of a fraction part, to control the input data of the fraction part so as to periodically change the input data of the fraction part according to a predetermined period corresponding to a value of the input data of the fraction part, and to output data of a controlled fraction part; and

a first adder operable to add an input data of an integral part to the data of the controlled fraction part outputted from said fraction part control circuit, and to output resultant addition data to said variable frequency divider as the input data corresponding to the number of frequency division,

wherein said fraction part control circuit is a plural-(n + m)-th-order delta-sigma modulator circuit, said fraction part control circuit comprising:

a first delta-sigma modulator circuit;

a second delta-sigma modulator circuit; and

a natural-number-n-th-order differential circuit having a transfer function which is expressed by $(1-z^{-1})^n$ using a z-transformation for representing delay of one clock period as z^{-1},

wherein said first delta-sigma modulator circuit comprises:

a first integrator which is a natural-number-n-th-order integrator;

a first quantizer; and

a first feedback circuit,

wherein said second delta-sigma modulator circuit comprises:

a second integrator which is a natural-number-m-th-order integrator;

a second quantizer; and

a second feedback circuit,

wherein output data from said second quantizer of said second delta-sigma modulator circuit is inputted to said natural-number-n-th-order differential circuit,

wherein said fraction part control circuit further comprises:

a second multiplier operable to multiply output data from said first quantizer by the predetermined quantization step, and to output resultant multiplication data;

a subtracter operable to subtract the output data from said second multiplier from output data from said first integrator, and to output resultant subtraction data to said second delta-sigma modulator circuit;

a delay operable to delay the output data from said first quantizer in said first delta-sigma modulator circuit so as to be synchronized with a timing of output data from said natural-number-n-th-order differential circuit; and

a second adder operable to add the output data delayed by said delay to the output data from said natural-number-n-th-order differential circuit, and to output resultant addition data as output data from said fraction part control circuit.

Claim 2 (Currently amended) The frequency synthesizer apparatus as claimed in claim 1,

wherein said fraction part control circuit is a binary logic circuit, and

wherein a bit length indicating data less than a quantization step of said second quantizer in the output data from said second integrator is smaller than a bit length indicating data less than a quantization step of said first quantizer in the output data from said first integrator.